BLOCK LMS ADAPTIVE CARRIER RECOVERY PHASE LOCKED LOOP FOR HIGH SPEED QAM DATA TRANSMISSION SYSTEMS

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Abstract - This paper presents a system for adaptive carrier phase tracking which is a part of the receiver for QAM modems' signals. The basic module of this system is decision-directed second-order phase locked loop whose primary task is to compensate phase and frequency offset of the signal after equalization. Besides this, the system includes the adaptive phase jitter predictor which is essential for high-efficient performance in high-speed data transmission. The predictor updating is realized with the BLOCK LMS algorithm. This algorithm reaches the same performance as the standard LMS, but is much more convenient for DSP implementation because it consumes a shorter processing time.

1. INTRODUCTION

Quadrature amplitude modulation (QAM) modem signals for high speed data transmission systems over voiceband telephone channels show increased sensitivity to the phase jitter; with enlargement of the system efficiency number bit/s/Hz the error rate caused by phase jitter becomes higher. That was the reason why the well known decision-directed phase locked loop, which is a component of the adaptive passband equalizer [1], had to be substituted by a high-performance adaptive system for phase jitter suppression. The adaptive predictor for the phase jitter tracking, patented by Gitlin [2], has provided good ideas for building carrier recovery systems that combine the desired convergence stability of the second-order decision phase locked loop (PLL) and the phase jitter suppression capability of the adaptive predictor. The cascade combination of these two modules has originally improved by Gooch [3] who has designed the adaptive phase locked loop (APLL). Additionally, it is important to note a similar solution where the bank of adaptive infinite impulse response filters [4] is used instead of adaptive finite impulse response filter [2].

In this paper we present one solution of the adaptive phase locked loop. The complexity implementation problem of the APLL is pointed out because of a large number of taps of the adaptive predictor we need for the phase jitter efficient suppression. Namely, simulations and experimental measurements [5], [6] have shown that the APLL has much more difficulties for low frequencies phase jitter. Particular problems come from phase jitter components at the ringing frequency (20 Hz in USA, 25 Hz in Yugoslavia). This problem can be solved using the BLOCK LMS algorithm [6], [7] which is more practical for DSP implementation than the standard LMS algorithm [8]. In this paper we shown just a part of results for 128QAM and 32QAM systems (CCITT V.33 and V.32) that illustrate performances of the BLOCK LMS phase locked loop.

In Section 2. we described a model of the signal at the input of the carrier recovery system. A review of the PLL, adaptive predictor and APLL is given in Section 3. The BLOCK LMS algorithm is introduced in section 4. and results are provided in Section 5.

2. SIGNAL AT THE INPUT OF THE CARRIER RECOVERY SYSTEM

The block diagram of the adaptive receiver for QAM signals is shown in Fig. 1. It is assumed that transmission is ideal except for the phase impairments of the carrier at the output of the equalizer. So, taking this model, the signal at the input of the demodulator is given with

$$Y(n) = D(n)\exp[j(\omega_c nT + \varphi(n))] + \eta(n) \quad (1)$$

where $D(n)$ is the two dimensional symbol transmitted in $t=nT$, ω_c is the known carrier frequency, T is the symbol interval, $\varphi(n)$ is the uncompensated carrier phase and $\eta(n)$ is the additive white Gaussian noise.

The transmission system, as it is known, introduces different types of phase degradation and the convenient model of the carrier phase is [1]

$$\varphi(n) = \varphi_o + \Delta nT + \mu(n) \quad (2)$$

where the constant phase offset is φ_o, the constant frequency offset is Δ and the phase jitter is $\mu(n)$. Generally, the phase jitter is a random signal but, taking into account the fact that the most typical sources of the phase jitter are the power line harmonics and/or ringing frequencies, the phase jitter signal can be defined with

$$\mu(n) = \sum_{j=1}^{J} A_j \sin(2\pi f_j nT) \quad (3)$$

where A_j and ω_j are amplitude and frequency of the phase jitter, respectively.

3. DESCRIPTION OF THE CARRIER RECOVERY SYSTEM

3.1 Conventional PLL

The PLL is derived from the first-order decision-directed phase lock loop originally designed by Falconer [1]. The block diagram of the PLL and its linear model are shown in Fig. 2. The PLL includes the angular error calculator, phase loop filter and numerically controlled oscillator. The angular error is an angular offset of a complex symbol after demodulation with respect to the transmitted symbol and it is determined with

$$\psi_n = \mathrm{Im}(Z_n / D_n) = \frac{1}{|D_n|^2} \mathrm{Im}\,(Z_n D_n^*) \qquad (4)$$

where Im and * denote the imaginary part of its argument and conjugate-complex value, respectively.

The linear model is valid for small values of the phase error so we can use approximation $\sin[\varphi(n)-\hat{\varphi}(n)]+\theta(n) \cong \varphi(n)-\hat{\varphi}(n)+\theta(n)$, where $\theta(n)$ is noise after demodulation. In this case the transfer function of PLL is

$$H_{PL}(z) = \frac{\hat{\varphi}(z)}{\varphi(z)} = \frac{z^{-1} H_p(z)}{1 + z^{-1} H_p(z)} \qquad (5)$$

where $\varphi(z)$ and $\hat{\varphi}(z)$ are the Z transformations of $\varphi(n)$ and $\hat{\varphi}(n)$, respectively. The transfer function of the phase loop filter is

$$H_p(z) = \frac{(a_1 + a_2) - a_1 z^{-1}}{(1 - z^{-1})^2} \qquad (6)$$

where coefficients a_1 and a_2 determine its passband.

The selection of the values of PLL coefficients is basically the problem of finding a compromise between the wide-band filter appropriate for phase jitter tracking and the narrow-band filter desired for better noise rejection. Fig. 3. shows several plots of the magnitude of H_{PL} using different values for coefficients a_1 and a_2. These values are optimized to reach the fastest convergence time of phase error for a given noise bandwidth [6]. The theoretical analyses and practical results show that the PLL attains stable convergence for phase and frequency offsets. On the other side the spectral content of the phase jitter is variable so we must use the carrier recovery system with adaptive parameters and which will minimize noise effects at the loop output.

3.2. Phase jitter predictor and APLL

The phase jitter predictor and its realization are shown in Fig.

4. The phase estimate is given as a weighted sum of previous values of the phase

$$\hat{\varphi}(n) = \sum_{i=0}^{N-1} g_i \, \varphi(n-i) \qquad (7)$$

where g_i, $i=0,\ldots N-1$, are adaptive coefficients
The predictor is a finite impulse response filter whose transfer function is

$$G(z) = g_0 + g_1 z^{-1} + g_2 z^{-2} + \ldots + g_{N-1} z^{-(N-1)} \qquad (8)$$

As we can see in Fig.4., the sum of phase error $\psi(n)=\varphi(n)-\hat{\varphi}(n)+\theta(n)$ and phase estimate $\hat{\varphi}(n)$ is applied at the input of the predictor instead of signal $\varphi(n)$. Namely, this signal is unknown for a receiver and it is approximated with noisy phase estimate $\varphi(n)+\theta(n)$.
The efficiency of the phase jitter suppression depends on its severity and on the length of adaptive predictor. Generally, a longer predictor will provide a better synthesis of the phase jitter signal. In the case when there is no phase jitter the predictor coefficients will fluctuate around zero values so we should not expect a noise enhancement.
This adaptive predictor, as we noted above, is used in combination with the conventional PLL for designing a high-performance system for carrier phase tracking. The straightforward connection of the PLL (Fig.2a) and the adaptive predictor (Fig.4b) in series is not practical because a redundant function will appear (slicing, angular error calculation, multiplication). The solution introduced by Gooch [3] overcomes the mentioned problem: the adaptive phase lock loop which approximates series of the PLL and the desired predictor (Fig.4a). The APLL is shown in Fig. 5.
The phase error transfer function of the APLL is given with

$$H_{AP}(z) = \frac{\varphi(z) - \hat{\varphi}(z)}{\varphi(z)} = [1 - z^{-1}G(z)] \frac{(1 - z^{-1})^{-2}}{1 + (a_1+a_2)z^{-1} - a_1 z^{-2}} \qquad (9)$$

where the first term in square brackets is the error transfer function of the adaptive predictor and the second term is a corresponding function of the PLL. In function (9) it is important to note that the poles of the PLL are not changed with adding of the adaptive predictor. This indicates that the APLL maintains the convergence stability obtained the PLL.

4. BLOCK LMS ALGORITHM

The predictor adaptation can be done, as we said, using the standard LMS algorithm. However, taking into account the fact that better phase jitter suppression requires a great number of coefficients, it is clear that the complexity problem will appear. As a measure of a sufficient predictor length, it is practical to use the relation stating the predictor should span at least 1/2 of the period of incoming sinusoid [4], i.e.

$$N = k\ \pi/2\pi f_j\ T, \quad k = 1,2... \tag{10}$$

The above relation shows that for the phase jitter at lower frequencies the length of the predictor must be longer. For instance, for sinusoides 20, 50 or 300 Hz and baud rate 2400 the predictor lengths should be 60, 24 and 4, respectively.

The described problem can be mitigated by applying the BLOCK LMS algorithm which is less complex for the DSP implementation than the LMS algorithm. The BLOCK LMS algorithm is given with

$$g^i(n+L) = g^i(n) + \rho_L/L \sum_{m=1}^{L} \psi(n-m+1)\ \phi(n-m-i), \quad i=0,...N-1 \tag{11}$$

where ρ_L is adaptation constant and L is block length.

The block length L determines the adaptation period for each coefficient and, at the same time, it is the length of a data block which we use for gradient estimation. As we can see from (11), for L=1 the BLOCK LMS becomes the standard LMS algorithm

$$g^i(n+1) = g^i(n) + \rho_1\ \psi(n)\ \phi(n-i-1), \quad i=0,...N-1 \tag{12}$$

The analytical and simulation results [6],[7] have shown the BLOCK LMS algorithm can reach the same convergence characteristics as the LMS if the following relation is valid

$$\beta_L = L\ \beta_1. \tag{13}$$

4.1 Algorithm for APLL

The complete algorithm for the APLL is given with (14)

a) $\psi(n) = \text{Im}[Z(n)\ D(n)^*]/E[|D(n)|^2]$ PHASE ERROR

b) $\hat{\theta}(n) = \hat{\theta}(n-1) + a_2[\psi(n) + \hat{\varphi}_2(n-1)]$ PLL

$\hat{\varphi}_1(n) = \hat{\varphi}_1(n-1) + \hat{\theta}(n) + a_1[\psi(n) + \hat{\varphi}_2(n-1)]$

c) BLOCK LMS ALGORITHM

$$g^i(n+L) = (1+\gamma)g^i(n) + \beta_B/L \sum_{m=1}^{L} \psi(n-m+1)\ \phi(n-m-i), \quad i=0...N-1$$

d) Shifting the delay line of predictor

e) $\hat{\varphi}_2(n) = \psi(n) + \hat{\varphi}_2(n-1)$ NEW INPUT DATA

f) $\hat{\varphi}_2(n) \doteq \sum_{i=0}^{N-1} g^i(n)\ \hat{\varphi}_2(n-i)$ PREDICTOR OUTPUT

g) $\hat{\varphi}(n) = \hat{\varphi}_1(n) + \hat{\varphi}_2(n)$ APLL OUTPUT

The symbol E in (14 a) denotes ensemble averaging.
It is important to note that normalization $1/|D(n)|^2$ in (4) is replaced by $1/E[|D(n)|^2]$ in (14a). The simulations have shown that the last method of normalization is more convenient because the variance of the phase error is smaller. In addition, in (14c) we introduced a small positive constant γ. This is the "leakage" [9] parameter important for stable convergence of the digital implementation, for the same reason as for fractionally spaced equalizers.

4.2 Implementation complexity

The BLOCK LMS algorithm is suitable for signal processors implementations because their architectures provide efficient multiplication with accumulation. Herein we examine the implementation with processor TMS320C25 which we used for modem V.32 [10]. We considered program modules for both algorithms and found the relations for the number of instruction cycles

$$\begin{array}{ll} \text{for LMS:} & 12 + 3N \\ \text{for BLOK LMS:} & 23 + N \end{array} \qquad (15)$$

where for the BLOCK LMS algorithm we set L=N.

5. TESTING RESULTS AND CONCLUSIONS

Herein we present testing results which illustrate the efficiency of the APLL with respect to sinusoidal phase jitter. The simulations were carried out for 128QAM system where we had the T/2 passband equalizer with 48 coefficients. Fig. 6 shows the phase error convergence for the APLL with the PLL bandwith 20 Hz and the adaptive predictor with N=64 coefficients. The flat channel introduced the phase jitter at the frequency of 20 Hz and the amplitude of 10 deg. The adaptation constants were selected to satisfy the relation (13), $\beta_L=2^{-\sigma}$, $\beta_1=2^{-1}$ and L=32. It is important to point out that the train sequence was in accordance with CCITT V.33 and that we used the following timing for different modules of the equalizer:

1. Segment "A,B,A,...B" - the PLL was turned on
2. Training segment - equalizer updating
3. Predictor updating started 250 T after turning the equalizer on.

In Fig. 6 we can see that the BLOCK LMS algorithm shows the same convergence of the phase error as the standard LMS.

The efficiency of the APLL in the case of multi-harmonics phase jitter is illustrated in Fig. 7. This plot shows the signal constellation of the 128QAM signal at the output of the T/2 equalizer. The signal was sampled at the period of 1700 symbol intervals immediately after training. In this case the signal-noise ratio was 35 dB and the phase jitter frequencies and amplitudes were $f_1=50$, $f_2=100$, $f_3=150$, $f_4=300$ Hz and $A_1=8$, $A_2=6$, $A_3=4$, $A_4=2$ deg. The described APLL is also used in modem V.32 which is implemented on TMS320C25. Herein we select some experimental results obtained under the following conditions: flat channel, signal level $R_x=-20$ dBm, phase jitter 60 Hz and rate 9600 bit/s. Fig. 8. shows the error rate for different amplitudes of the phase jitter. First, we turned off the adaptive predictor so the carrier recovery system was reduced to the conventional PLL. The given results indicate the high level of the residual phase jitter and because of that increased error rate. Also, it is clear that PLL is not appropriate for the 32QAM system. After that we repeated the measurements for the APLL (predictor turned on) and obtained very close results independent of amplitude of the phase jitter.

REFERENCES

[1] Falconer D.D., "Jointly Adaptive Equalization and Carrier Recovery in Two-Dimensional Digital Communication Systems," B.S.T.J.,Vol.55, No.3, March 1976.

[2] Gitlin R.D., "Adaptive Phase-Jitter Tracker," United States Patent, Patent number 4,320,526, March 16, 1982.

[3] Gooch R.P., M.J.Ready, "An Adaptive Phase Lock Loop For Phase Jitter Tracking," 1988 Maple Press, pp.437-441.

[4] Cupo R.L., Gitlin R.D.,"Adaptive Carrier Recovery Systems for Digital Data Communications Receivers," IEEE Journal on Selected Areas in Communications, December 1989.

[5] Tretter S.A. "Improving the Convergence of the Phase Jitter Predictor," Penril Data Comm private, August 1989.

[6] Krsti} R.V., "Optimal Channel Equalization and Carrier Phase Estimation in Data Transmission System," M.S. thesis, Faculty of Electrical Engineering University of Belgrade, 1990.

[7] Clark G.A., S.K.Mitra, S.R.Parker, "Block Implementation of Adaptive Digital Filters," IEEE Trans. on ASSP, June 1981

[8] Widrow B. S.D.Stearns, "Adaptive Signal Processing" Prentice-Hall, 1985.

[9] Gitlin R.D., H.C.Meadors, and S.B.Weinstein, "The Tap-Leakage Algorithm: An Algorithm for the Stable Operation of a Digitally Implemented, Fractionally Spaced Adaptive Equalizer," B.S.T.J., October 1982., pp. 1817-39.

[10] Project: V.32, full-duplex two-wire 9.6 Kbps modem Institut Mihajlo Pupin Yugoslavia, Penril Data Comm USA , 87.

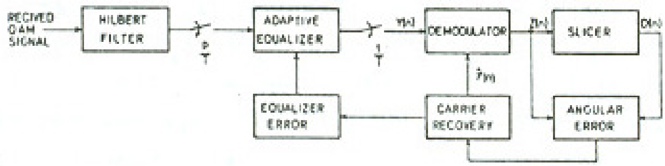

Fig. 1. Basic block diagram for QAM receiver

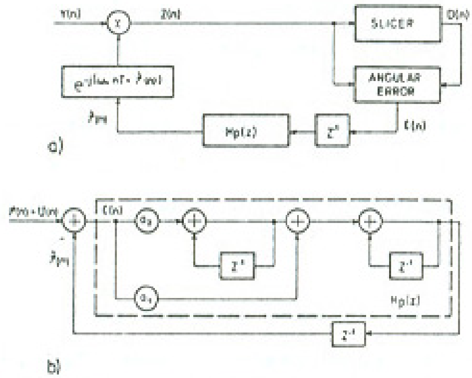

Fig. 2. PLL: a) Block diagram.
b) Equivalent linear model

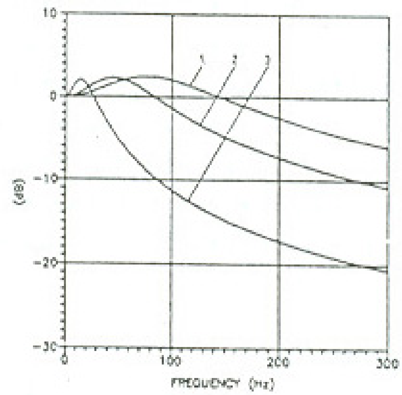

Fig.3. PLL magnitude response for: 1) a_1=0.2947, a_2=0.0512
2) a_1=1890 , a_2=0.0197
3) a_1=0.0674, a_2= 0.023

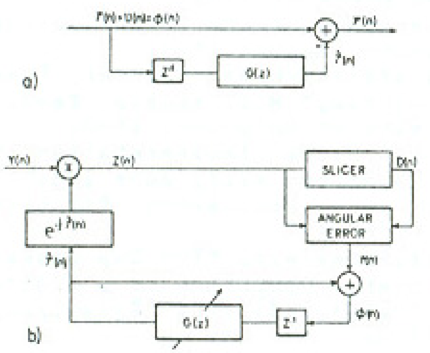

Fig. 4. Phase jitter adaptive predictor a) Desired model
b) Realization

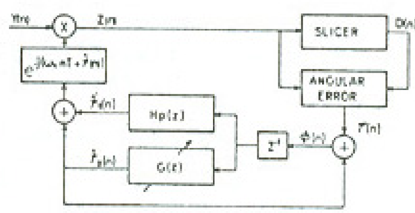

Fig. 5. Adaptive phase locked loop (APLL)